The design of GALFA Quadrature Downconverter Controller Board

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Specifications:

The GALFA Quadrature Downconverter Controller (QDC) interfaces the GALFA spectrometer computer and the analog QD boards. It is desired that for IF input levels between -25dBm to -10dBm, the output power from the analog QD is constant (about 0dBm). The GALFA spectrometer computer will sense the power level at the output, and using a DAC, it will adjust the gain on the analog QD board. The QDC board is designed to regulate and supply power up to 16 analog QD boards. The QDC board will need to translate RS232 logic levels sent from the computer to TTL logic levels used by the DACs.

Block Diagram and Schematic:

Fig.1 shows the Orcad *Capture CIS* schematic of QDC board. The CLK and DATA RS232 logic level inputs come through the DSUB-9 connector on pin 4 and 7, respectively. A 10uF capacitor is used to remove the high frequency component in the 5V power supply. A light diode in series with a 150Ω resistor is used to show that the power is connected to the board.

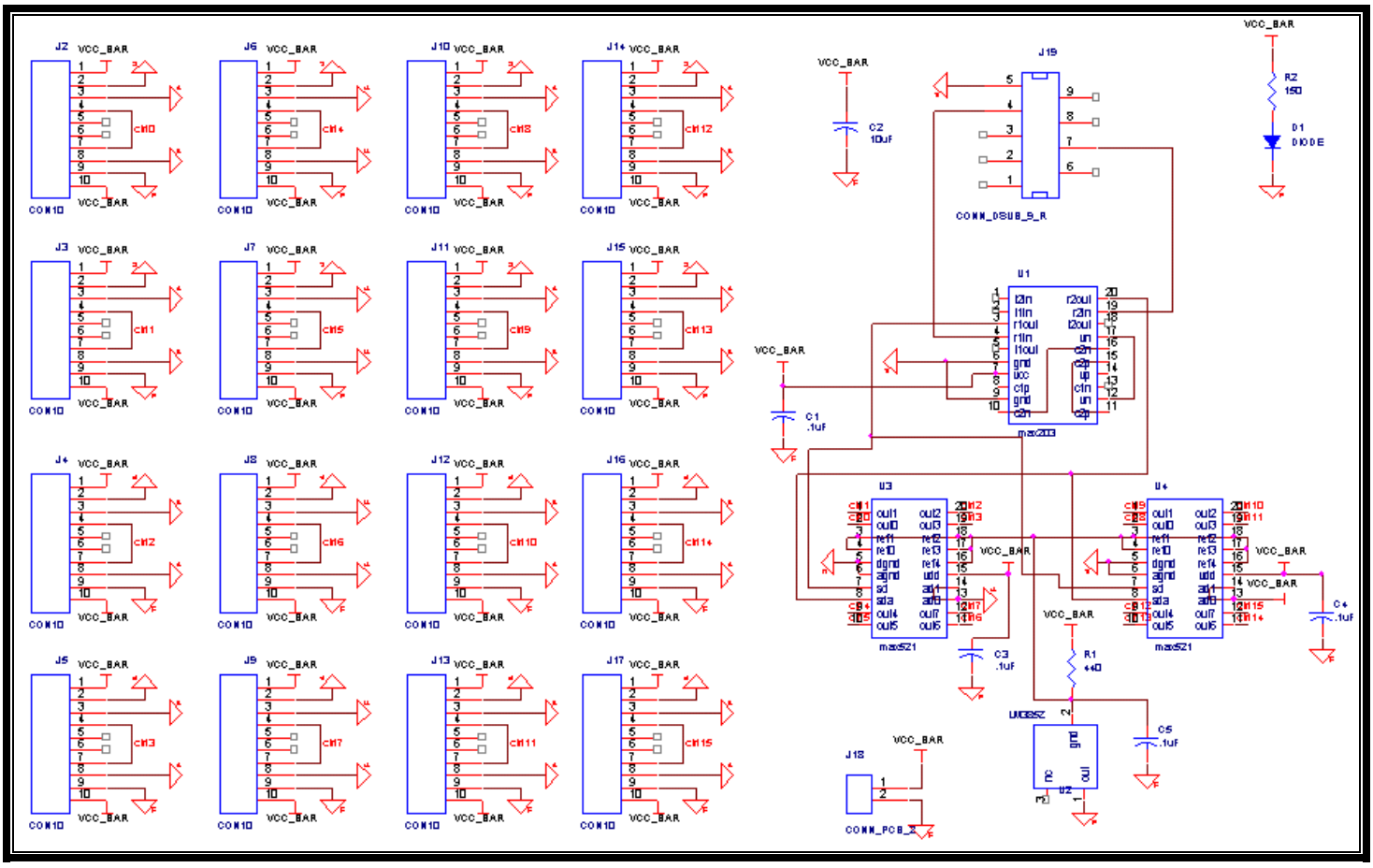

Figure 1: QDC schematic.

Fig.2 shows the pin configuration and typical operation circuit for MAX203 (through-hole package). Pin 7 is connected to 5V power supply and decoupled with 0.1uF cap. Pins 4 and 19 are connected to CLK and DATA RS232 inputs, respectively. Pins 3 and 20 are the TLL outputs from pin 3 and 20, respectively. Pin 10 is tied to pin 16, pin 11 is tied to pin 15, and pin 12 is tied to pin 17. Pins 6 and 9 are grounded. Pins 1, 2, 5, and 18 are unused. The data sheet for MAX203 can be found at: http://pdfserv.maxim-ic.com/en/ds/MAX200-MAX213.pdf .

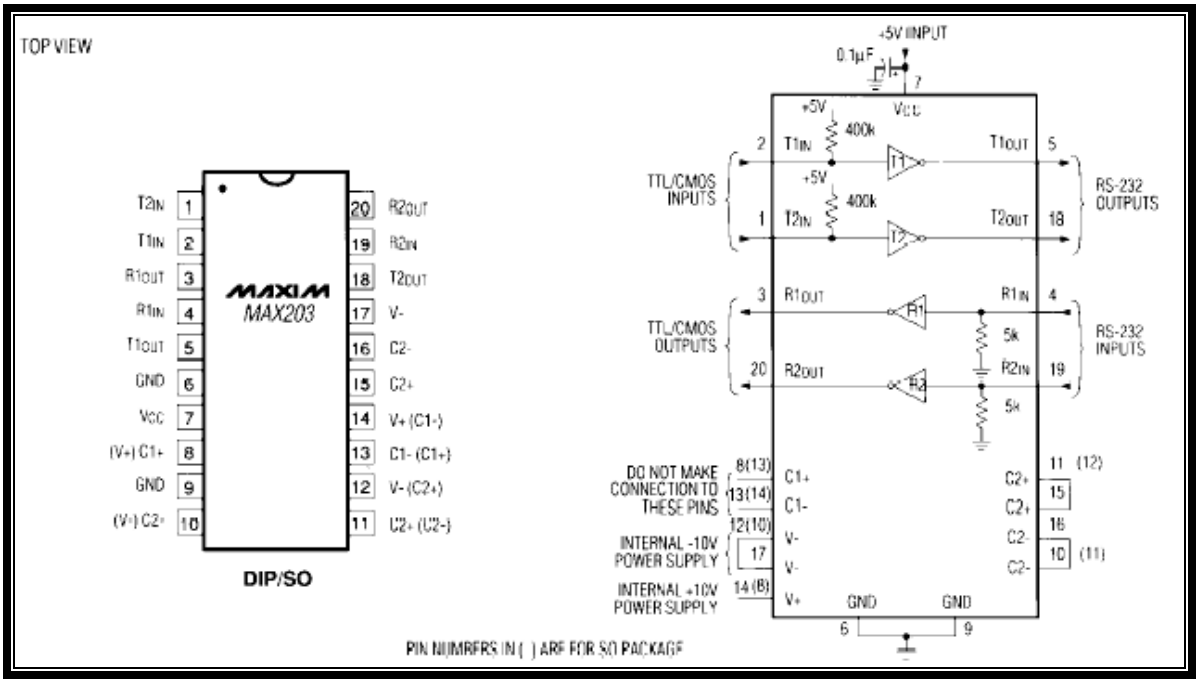

Figure 2: MAX203 pin-out

Fig. 3 shows the pin-out of MAX521 8-channel DAC. Pin 15 is connected to 5V power-supply and is decoupled using 0.1uF capacitor. Pins 5 and 6 are grounded.

Pin 3, 4, 16, 17, and 18 are connected to 1.5V voltage reference that limits the analog output of the DAC to 1.5V (the voltage control range on the analog QD board is $0.2V_{max\ gain}$ to $1.2V_{min\ gain}$).

Pin 13 and 14 set the address of the MAX521. The pins 13 and 14 of left MAX521 chip (U3) are grounded (and therefore its address is 00). The pins 13 and 14 of right MAX521 chip (U4) are tied to power-supply (and therefore its address is 11).

Pins 1, 2, 9, 10, 11, 12, 19, and 20 are the analog outputs of the MAX521. Each analog output is tied to pin 4 and 7 of the ten pin connector. Table 1 shows the correspondence of 16 analog DAC outputs to 16 ten pin connectors.

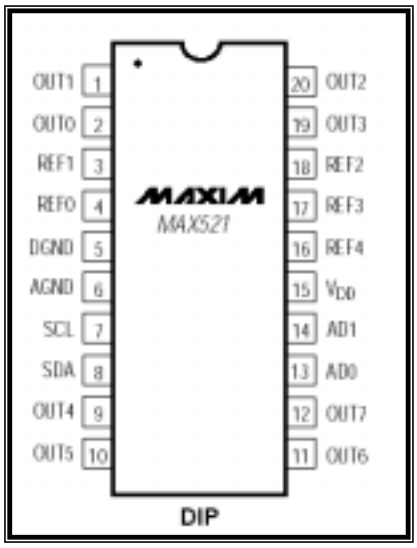

Figure 3: MAX521pin-out

Table 1: 16 DAC outputs to 16 ten pin connectors' correspondence.

Pin	Schematic MAX521 reference	Net Alias	Schematic 10 pin connector reference	Board layout/silk screen reference
1	U3	ctrl1	J3	0b
2	U3	ctrl0	J2	0a
9	U3	ctrl4	J6	2a
10	U3	ctrl5	J7	2b
11	U3	ctrl7	J9	3b
12	U3	ctrl6	J8	3a
19	U3	ctrl3	J5	1b
20	U3	ctrl2	J4	1a
1	U4	ctrl9	J11	4b
2	U4	ctrl8	J10	4a
9	U4	ctrl12	J14	6a
10	U4	ctrl13	J15	6b
11	U4	ctrl15	J17	7b
12	U4	ctrl14	J16	7a
19	U4	ctrl11	J13	5b
20	U4	ctrl10	J12	5a

The data sheet to MAX521 can be found

at: http://pdfserv.maxim-ic.com/en/ds/MAX520-MAX521.pdf .

The 1.5V voltage reference is created using 1.5V precision LM385Z diode from National Semiconductor. The LM385Z diode is reverse biased in series with 440Ω resistor. A 0.1uF cap is used to cancel high frequency jitter at the output of the voltage reference. Pin 2 is tied t the 440Ω resistor and 0.1uF capacitor, pin 1 is tied to ground, and pin 3 is left open. The data sheet for LM385Z can be found at: http://space.auburn.edu/CHS/mag/LM185-ADJ.pdf .

Layout:

Fig. 4 shows QAC board layout. All chips have DIP package and all passive parts are through hole. All decoupling capacitors are placed as close to power-supply pins as possible.

The positive power supply is tied to 150x150 mil^2 square pad. The negative ground it tied to 150 mil diameter round pad. The pads are separated by 100 mils. The power is routed to chips and 10 pin connectors via 80 mil traces.

The DAC output voltages are routed via 25 mil trances to 10 pin connectors. Top copper layer is used for vertical traces, and bottom copper layer is used for horizontal traces.

The MAX521 chips were bought from Newark Electronics. The MAX203 chips were bought from Avnet.

The final board dimensions are 3.4 by 4.3 inches.

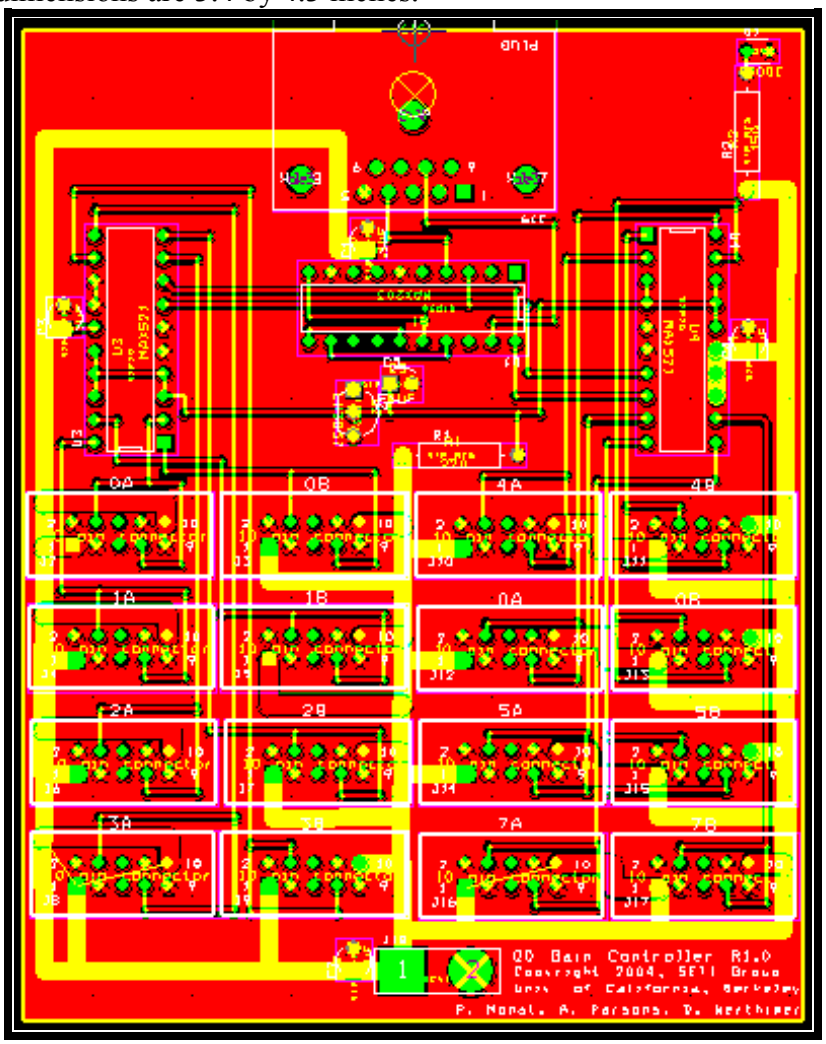

Figure 4: QDC layout

If you have any questions about this report, please e-mail me: pmonat@umich.edu